REMARKS

Claims 1-29 are pending in the present application. Claim 13 was amended. No claims were canceled or added. Reconsideration of the claims is respectfully requested.

I. Rejection under 35 U.S.C. § 102, Anticipation

The Examiner has rejected Claims 1, 5, 6, 9-11, 13, 14, 19 and 23-25 under 35 U.S.C. § 102(e), as being anticipated by U. S. Patent No. 6,775,084, to Ozdemir et al. This rejection is respectfully traversed.

II. Rejection under 35 U.S.C. § 103, Obviousness

The Examiner has rejected Claims 2, 7, 8, 12, 20-22 and 26-28 under 35 U.S.C. § 103(a), as being unpatentable over Patent No. 6,775,084, in view of U. S. Patent No. 6,021,013, to Albrecht et al.

Claim 15 was rejected under 35 U.S.C. § 103(a), as being unpatentable over Patent No. 6,775,084 in view of U. S. Patent No. 6,028,488, to Landman et al.

Claim 16 was rejected under 35 U.S.C. § 103(a), as being unpatentable over Patent No. 6,775,084 in view of U.S. Patent No. 6,389,090, to Zortea et al.

Claims 17 and 18 were rejected under 35 U.S.C. § 103(a), as being unpatentable over Patent No. 6,775,084 in view of U. S. Patent No. 5,995,306, to Contreras et al.

Claim 29 was rejected under 35 U.S.C. § 103(a), as being unpatentable over Patent No. 6,775,084 in view of U. S. Patent No. 6,075,666, to Gillingham et al.

Claims 3 and 4 were rejected under 35 U.S.C. § 103(a), as being unpatentable over Patent No. 6,775,084 in view of Abe (Derwemt Acc-No. 1992-167403).

Each of the above rejections under 35 U.S.C. § 103(a) is respectfully traversed.

III. Purpose of Applicants' Invention

Applicants' invention generally pertains to an adaptive tape speed arrangement or system. In such arrangements the speed of moving data storage tape is varied, in order to match variations in the data exchange rate of an associated host system. Generally, arrangements of this

type require a timing signal to coordinate the moving tape speed with the data exchange rate. However, prior art arrangements of the above type have been adversely affected by timing errors associated with the timing signal. Accordingly, Applicants' invention is provided, in order to overcome these deficiencies of the prior art. The above teachings of Applicants are set forth in the application, such as at page 2, line 6 through page 3, line 6:

> Adaptive tape speed systems attempt to remedy the situation by varying the tape speed to match the data rate to/from the host. U.S. Patent No. 5,892,633, to Ayres, et al., entitled "Dynamic Control of Magnetic Tape Drive," describes one such system, which relies on a buried (or embedded) servo pattern, normally used to align the read/write head with the tape, to determine the speed of the tape at a given moment and adjust the data rate of data being read or written to/from the tape to match the tape speed. U.S. Patent No. 6,122,124, to Fasen, et al., entitled "Servo System and Method with Digitally-Controlled Oscillator," also uses a servo pattern to measure the tape speed and adjust the data rate, except that a timing-based servo is used instead of a buried servo.
>
> Two problems exist with these servo based methods. The first is that if the read/write head is shifted off track center (which is a common occurrence), the timing signals experience phase variations, which affects the quality of the generated clock signal, and thus could cause timing errors. The second is that the low frequency nature of these servo signals requires large multiplication factors to achieve the clock frequencies of interest. This large multiplication factor also has the potential to cause phase variations affecting the quality of the generated clock signal. As the tape drive transfer rates increase, the problems become more acute. What is needed, then, is an adaptive media speed storage device that uses a modified pattern designed specifically for timing measurements.

IV. Essential Features of Applicants' Invention

Applicants' Claim 1 currently reads as follows:

> 1. A method of establishing a data transfer rate between a moving storage medium and a read/write device, said method comprising the steps of:
>
> reading successive reference regions on the moving storage medium to derive a timing signal having a frequency that varies directly with variations in the speed of the moving storage medium;
>
> processing the timing signal to provide a clock signal having a frequency that is a function of the timing signal frequency, and thereby represents the speed of the storage medium; and
>
> using the clock signal to determine the rate for writing data to the moving storage medium, so that said rate is proportional to the speed of the moving storage medium.

Essential features of Applicants' invention, as exemplified by Claim 1, are illustrated by **Figures 1** and **5** of the application, together with the following sections of the specification, such as at page 8, line 6 through page 9, line 7, page 12, lines 11-17 and page 13, lines 11-17. These excerpts of the application, which are set forth below, clearly teach use of a read/write head **106** to read successive reference regions **308** on a moving storage medium, such as magnetic tape **108**, in order to derive a timing signal **116** having a frequency that varies directly with the speed of the moving storage medium. This is an essential feature of Applicants' invention, and is necessary to allow data to be written to the magnetic tape **108** at any speed that matches the tape speed, as taught by Applicants at page 8, lines 12-15. This essential feature, also recited as the reading step of Applicants' Claim 1, is further supported at page 12, lines 11-14.

Figure 5, together with teachings at page 13, lines 11-17, emphasizes a further essential feature of the invention, namely that successive reference regions **308** must be read, in order to derive the required timing signal. **Figure 5** shows timing signal **116** comprising successive waveforms **312**, each resulting from a different successive reference region **308**. If only one reference region **308** of Applicants' disclosure was read, only one waveform **312** would be produced. In this event, there would be no timing signal **116**, having a frequency that varies directly with variations of storage medium speed. The required feature of reading successive reference regions to derive a timing signal is expressly recited in the reading step of Applicants' Claim 1.

The remaining steps of Claim 1 are taught in the application such as at page 9, lines 4-7. These steps include processing the timing signal **116** to provide a clock signal **120** that represents the speed of the storage medium, and using the clock signal to determine a rate for writing data to the moving storage medium that is proportional to the medium speed. **Figures 6** and **7** of the application, together with page 13, lines 19-24 and page 15, lines 3-9 further support the processing step recited in Applicants' Claim 1. The application at page 15, lines 27-29 further supports the using step of Claim 1. These excerpts are also set forth hereinafter.

FIG. 1

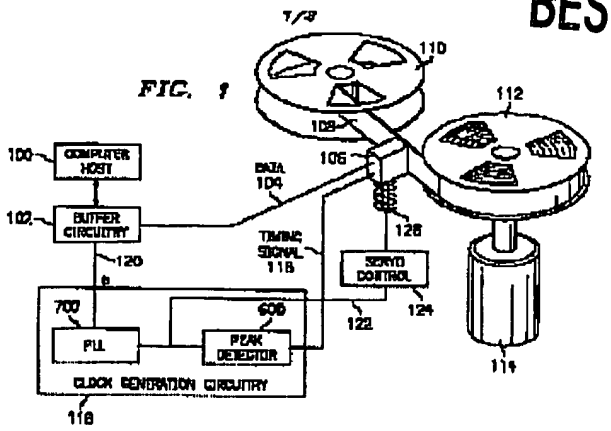
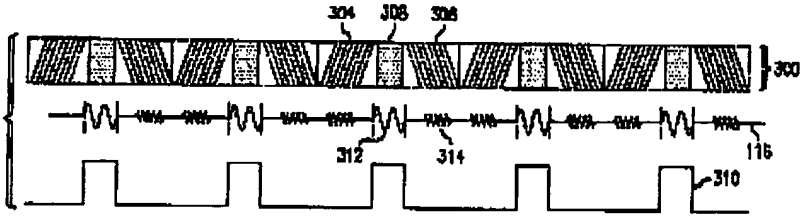


FIG. 5



Magnetic tape **108** moves from source spool **110** to take-up spool **112** in a pulley action from force applied by motor **114**. Source spool **110** and take-up spool **112** may exist separately, or may be incorporated into an integrated package, such as a tape cartridge or cassette. Motor **114** may operate at any of a continuous range of possible speeds. The present invention allows data to be written to magnetic tape **108** at a speed that matches the speed of motor **114**. In this way, motor **114** can be sped up or slowed down as needed.

For example, if buffer circuitry **102** receives a large amount of data that must be written to magnetic tape **108**, motor **114** can be sped up to match the flow of data into buffer circuitry **102**. If the amount of data to be written is low, motor **114** can be slowed down. Conversely, computer host **100** is able to read a large amount of data at one time, motor **114** can be sped up to accommodate computer host **100**'s need for data. If computer host **100** cannot process a large amount of data at present, motor **114** can be slowed down to match the current capacity of computer host **100**.

As magnetic tape **108** moves in relation to read/write head assembly **106**, read/write head assembly **106** reads a timing signal **116** from reference regions

written on magnetic tape **108**. This timing signal will increase or decrease in frequency in direct relation to the change in tape speed.

Clock generation circuitry **118** processes timing signal **116** to generate a clock signal **120** that may be used to time the reading and writing of data **104** by buffer circuitry. (Emphasis added) **(Page 8, line 6 through page 9, line 7)**

As the references regions pass by read/write head assembly **106** and are read, a timing signal (**116** in **Figure 1**) is produced with a frequency that matches the frequency at which the reference regions are read. A vertical reference region, such as reference region **308** is preferable to diagonal regions **304** and **306** for generating a timing signal. (Emphasis added) **(Page 12, lines 11-17)**

Figure 5 is a diagram showing the relation between a servo track (**300**) containing reference regions (e.g., **308**), and the timing signal (**116**) and processed timing signal (**310**) derived therefrom. As each reference region (e.g., **308**) is read by read/write head assembly **106** (**Figure 1**), a corresponding waveform **312** is read from magnetic tape **108**. **(Page 13, lines 11-17)**

Peak detecting read channel **600**, shown in **Figure 6**, processes timing waveforms such as waveform **312** and produces processed timing signal **310**, which is used to enable the circuit illustrated in Figure 7. The result of **Figure 7** is a clock signal that is phase-locked to signal **312**. **(Page 13, lines 19-24)**

Figure 7 is a block diagram of a phase-locked loop (PLL) that may be utilized in a preferred embodiment of the present invention. The input to the phase locked loop is reference frequency **702**, which is fed into phase detector **704**. In a preferred embodiment, reference frequency **702** is the processed timing signal from output **616** of peak-detecting read channel **600** (**Figure 6**). **(Page 15, lines 3-9)**

Output **716** drives data transfer clock signal **120**, which is used by buffer circuitry **102** to time reading and writing operations.). **(Page 15, lines 27-29)**

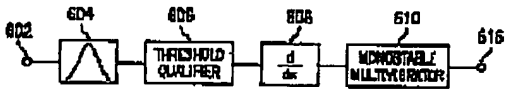


FIG. 6

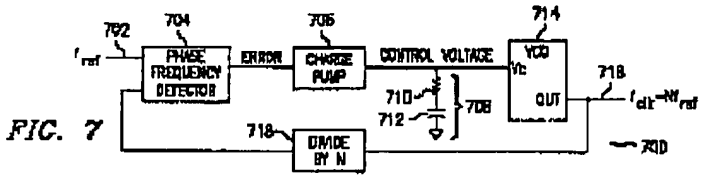


FIG. 7

V. Rejection of Claim 1

In the Final Office Action, the Examiner stated the following in rejecting Applicants' Claim 1 under 35 U.S.C. §102(e):

> 2. Claims 1, 5, 6, 9-11, 14, 19 and 23-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Ozdemir et al. (US Patent No. 6,775,084).
>
> Regarding Claim 13, Ozdemir et al. teaches an apparatus, comprising:
>
> A first read head disposed to reference regions from a moving storage medium, which is moving relative to the first read head, to generate a timing signal (See Fig. 1, Element 18);
>
> A phase detector having an input, a second input and an output, the timing signal being coupled to the first input of the phase detector (Fig 1, Element 26); and
>
> A voltage-control oscillator having an input and an output, the output of the phase detector being fed into the control input of the voltage control oscillator, and the output of the voltage control oscillator being coupled to the second input of the phase detector, to form a phase lock loop wherein the voltage control oscillator is locked to the timing signal to generate a signal representing the data transfer rate (Fig. 1, Elements 24 (which is the phase lock timing loop according to Col. 3, L. 21-25 according to Ozdemir et al. and Element 12, which is the voltage control oscillator or VCO. See also description of Fig. 1).
>
> Method claim (1) is drawn to the method of using the corresponding apparatus claimed in claim (13). Therefore method claim (1) corresponds to apparatus claim (13) and is rejected for the same reasons of anticipation as used above.

Final Office Action dated November 10, 2005, pages 2-3

VI. Principal Teachings of Ozdemir Reference

Figure 1 of Odzemir shows a read head 18 disposed to read a disk 16, and to generate a read signal representing data stored on respective sectors of the disk. Figure 1 further shows a

read circuit 20 that samples the read signal by means of a sample clock. As taught at col. 2, lines 1-14, at each sector of disk 16, read head 18 reads a preamble comprising a bit pattern stored at the beginning of the sector. While reading the preamble, read head 18 generates a sinusoid, wherein peaks and zero crossings of the preamble sinusoid correspond to data points of the read signal, and to the centers of data windows 34 shown in Figure 2. Each data point is the portion of the read signal that head 18 generates while positioned over a data storage location on the surface of disk 16.

At col. 2, lines 20-23 Odzemir further teaches that it is necessary to align the read signal and the sample clock during both the preamble and data portions of the read signal. Alignment, as used in Odzemir, refers to eliminating phase difference between the read signal and sample clock. In order to overcome certain drawbacks with prior art alignment practices, Odzemir teaches, such as at col. 3, lines 35-50, an arrangement which provides an initial coarse alignment between the read signal and the sample clock. This allows a shortening of the disk sector preamble and a corresponding increase in the data-storage density of a disk, which appears to be a central purpose of the Odzemir reference.

In Odzemir, the only timing signal discussed is the sample clock associated with read circuit 20. Clearly, the sample clock signal is in no way derived by reading successive reference regions on a moving storage medium, as required by Applicants' Claim 1. Odzemir, in fact, does not disclose how the sample clock thereof is derived. The concern in Odzemir is only to eliminate phase difference between the sample clock and the read signal. Moreover, Odzemir provides only perfunctory teaching in regard to movement of disk 16 and read head 18, and certainly does not teach that any such movement is of variable speed. At col. 12, lines 21-24, Odzemir states only that a motor 124 rotates disks 116 and maintains them "at the proper rotational speed." Clearly, Odzemir does not teach that such speed is variable.

Figure 1 of Odzemir, as well as sections thereof at col. 1, line 4 through col. 2, line 19, col. 3, lines 21-50, and col. 12, lines 21-24 are set forth below. These sections generally disclose the teachings of Odzemir discussed above, as well as portions thereof cited in the Office Action against Applicants' Claim 1.

Fig. 1
(Prior Art)

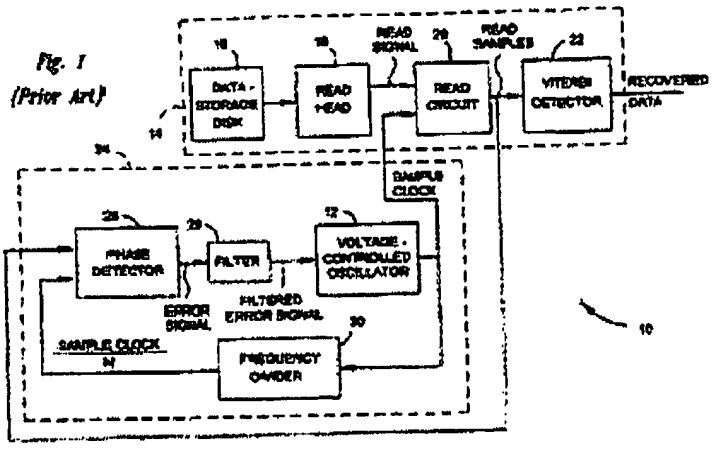


FIG. 1 is a block diagram of a conventional disk-drive read channel 10 having a voltage-controlled oscillator (VCO) 12, which may inject noise or transients into other circuits within the read channel 10 or elsewhere. The read channel 10 includes a read path 14, which includes a disk 16 for storing data, a read head 18 for reading the disk 16 and for generating a read signal that represents the read data, a read circuit 20 for sampling the read signal in response to a sample clock, and a Viterbi detector 22 for recovering the stored data from the samples of the read signal. The read channel 10 also includes a phase-locked timing loop 24 for generating the sample clock, for aligning the sample clock with the read signal such that the read circuit 20 samples the read signal at appropriate times, and for maintaining the alignment of the sample clock. The timing loop 24 includes a phase detector 26 for generating an error signal that represents the phase difference between the read signal and the sample clock, a filter 28 for filtering the error signal, the VCO 12 for generating the sample clock at a frequency indicated by the filtered error signal, and a frequency divider 30 for allowing the frequency of the sample clock to be greater than the data rate of the read signal. The read circuit 20 effectively closes the loop 24, i.e., couples the loop input to the loop output.

FIG. 2 is a timing diagram showing the desired alignment between the sample clock and the preamble portion of the

read signal. Referring to FIGS. 1 and 2, the preamble is a bit pattern stored at the beginning of every sector (individual sectors not shown) of the disk 16. The read channel 10 uses the preamble to calibrate the channel timing with respect to the read signal. While reading the preamble, the read head 18 generates a sinusoid (or an approximate sinusoid). The peaks and zero crossings of this preamble sinusoid correspond to the centers of respective data windows 34. During the subsequent data portion (not shown) of the read signal, the centers of the data windows 34 correspond to the data points of the read signal—the data points are the portions of the read signal that the head 18 generates while positioned directly over the respective storage locations on the surface of the disk 16. By aligning the sampling edges of the sampling clock with the peaks and zero crossings of the preamble sinusoid, these edges will be aligned with the centers of the data windows 34 during the data portion of the read signal, and thus will cause the read circuit 20 to sample the read signal at the data points.

(Col. 1, line 4 through col. 2, line 19)

But unfortunately, using a digital timing-recovery loop instead of the phase-lock timing loop 24 (FIG. 1) often requires a reduction in the data-storage density of the disk 16 (FIG. 1). The digital timing-recovery loop lacks a start-up circuit to provide a coarse alignment between the sample clock and the read signal. Without such a start-up circuit, the digital timing-recovery loop requires a longer time to acquire alignment than the timing loop 24, and thus requires a longer preamble. Because the preamble data pattern is stored at the beginning of each sector of the disk 16, the longer the preamble, the fewer the data bits that the disk 16 can store, and thus the lower the disk's data-storage density.

SUMMARY OF THE INVENTION

In one aspect of the invention, a circuit includes a buffer for receiving and storing two samples of a signal, and a phase calculation circuit for calculating from the samples a phase difference between one of the samples and a predetermined point of the signal.

Such a circuit can be used to decrease the alignment-acquisition time of a digital timing-recovery loop, and thus allows a shortening of the preamble and a corresponding increase in the data-storage density of a disk. In one application, the circuit determines an initial phase difference between a disk-drive read signal and a read-signal sample clock. The digital timing-recovery loop uses this phase difference to provide an initial coarse alignment between the read signal and the sample clock. By providing an initial coarse alignment, the recovery loop reduces the overall alignment-acquisition time.

(Col. 3, lines 21-50)

> desired data on the respective disks **116**. A spindle motor (SPM) **124** and a SPM control circuit **126** respectively rotate the disks **116** and maintain them at the proper rotational speed.

(Col. 12, lines 21-24)

VII. Ozdemir Does Not Disclose Essential Features of Claim 1

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F. 2d 831, 832, 15 U.S.P.Q. 2d 1566, 1567 (Fed Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F. 3d 1579, 1582, 21 U.S.P.Q. 2d 1031, 1034 (Fed Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. Kalman v. Kimberly-Clark Corp., 713 F. 2d 760, 218 U.S.P.Q. 781 (Fed Cir. 1983). Moreover, it is a fundamental principle of patent law that prior art must be considered in its entirety. **MPEP 2141.02.**

Applicants respectfully submit that Odzemir does not teach every element of the claimed invention arranged as they are in Claim 1. Specifically, Odzemir does not teach, in the over-all combination of Claim 1, any of the following Claim 1 features:

(1) Reading successive reference regions on a moving medium to derive a timing signal (hereinafter "Feature (1)")

(2) Reading successive reference regions on a moving storage medium to derive a timing signal having a frequency that varies directly with variations in the speed of the moving storage medium (hereinafter "Feature (2)")

(3) Processing the timing signal to provide a clock signal that is a function thereof and represents the speed of the storage medium (hereinafter "Feature (3)")

(4) Using the clock signal to determine the rate for writing data to the moving storage medium, so that said rate is proportional to the speed of the moving storage medium (hereinafter "Feature (4)")

A. **Odzemir Does Not Disclose Feature (1) of Claim 1**

As discussed above and as clearly shown by Applicants' **Figure 5**, it is critical to read successive reference regions **308** on a moving storage medium, in order to derive the timing signal of Applicants' Claim 1. If only one reference region **308** were to be read, only a single waveform pulse **312** would be generated, and there could be no timing signal.

In contrast, Odzemir teaches, such as at col. 2, lines 1-14, that a preamble bit pattern is stored at the beginning of every sector. When read head 18 arrives at the beginning of a sector, the read head reads the preamble and generates a sinusoid. The sinusoid acts to align edges of a sampling clock over respective data storage locations. When read head 18 arrives at the next disk sector, it reads that sector preamble, and then generates the same sinusoid, for use in aligning the same sampling clock. Thus, Odzemir clearly teaches that neither the read signal nor the sampling clock thereof is in any way changed or made different by reading successive sector preambles. The read signal and the sampling clock are the same after reading one preamble as they are after reading successive preambles. This fundamental teaching of Odzemir directs those of skill in the art away from the requirement of Applicants' Claim 1, that successive reference regions on a moving storage medium must be read, in order to derive a timing signal.

Applicants consider that the sector preambles of Odzemir do not show or suggest the reference regions of Claim 1. However, the sector preambles appear to be the features most pertinent to Applicants' reference regions that can be found in Odzemir.

B. **Odzemir Does Not Disclose Feature (2) of Claim 1**

As discussed above, Odzemir teaches that when read head 18 arrives at the beginning of any disk sector, the read head reads a preamble bit pattern and generates a sinusoid. The sinusoid is then used to align the sampling clock with the read signal and data storage locations of the disk sector. From these teachings, it is readily apparent that the speed of both disk 16 and read head 18, and of any motion therebetween, is completely irrelevant in the arrangement of Odzemir. In Odzemir, the preamble provided at the beginning of each sector serves to establish the needed relationship between the read signal and the sampling clock, after the read head reaches the sector. Moreover, both

of these signals are affected only after read head 18 has reached the beginning of a sector and starts to read the sector preamble. For these reasons, neither the speed of disk 16, nor the time required for read head 18 to move from one sector to the next, either affects or is of any concern to the Odzemir arrangement. Accordingly, Odzemir fails entirely to disclose Feature (2) of Applicants' Claim 1, that is, reading successive references on a moving storage medium to derive a timing signal having a frequency that varies directly with variations in the speed of a moving storage medium.

Moreover, Odzemir provides no teaching whatsoever in regard to variations of frequency of either the sampling clock or the read signal. Thus, Odzemir neither shows nor suggests that either of such signals could have "a frequency that varies directly with variations in the speed of a moving storage medium," as recited by Applicants' Claim 1.

C. Odzemir Does Not Disclose Feature (3) or Feature (4) of Claim 1

Since the speed of disk 16 is of no concern in the Odzemir arrangement, as discussed above, Odzemir clearly cannot show a clock signal that represents the speed of the storage medium, as recited by Feature (3) of Applicants' Claim 1. Odzmir also fails to disclose the Feature (3) recitation of processing a timing signal to provide a clock signal that is a function thereof. As for Feature (4) of Claim 1, Odzemir fails to disclose use of a clock signal to determine a rate for writing data to a moving storage medium that is proportional to the speed of the medium.

In regard to the Albrecht, Landman, Zortea, Contreras, Gillingham and Abe references, Applicants consider that none of such references, either alone or in any combination with one another or with Odzemir, overcome the deficiencies of Odzemir discussed above in regard to Applicants' Claim 1.

VIII. Claim 13 Distinguishes Over Ozdemir

Independent Claim 13 recites subject matter that is common to subject matter of Claim 1, and is considered to distinguish over the art including Odzemir for the same reasons given in support of such common subject matter.

Claim 13 is considered to further distinguish over Odzemir in expressly reciting that the speed of the moving storage medium is variable, in the over-all combination of Claim 13. The

Odzemir reference does not disclose any such feature.

IX. Claims 2-12 Distinguish Over Cited References

Claims 2-12 respectively depend from Claim 1, and are each considered to patentably distinguish over the art for the same reasons given in support thereof.

Claim 2 is considered to further distinguish over the art, including the cited Odzemir and Albrecht patents, particularly in reciting reference regions that extend in a second direction that is perpendicular to a first direction of storage medium movement, and in further reciting that respective reference regions are interleaved with timing-based servo regions that extend along diagonals with respect to the first and second directions. Albrecht, such as at col. 2, lines 55-67, teaches a track-following servo control system. The timing of pulses generated by the servo read head is decoded by appropriate circuitry to provide a speed invariant position signal used by the servo system to position the data heads over the desired data tracks on the storage media. Thus, Albrecht teaches away from the reference regions of Claim 2, which are provided to derive a timing signal that varies with storage medium speed variations, in accordance with Claim 1. The invention of Albrecht is only concerned with track patterns for use in positioning data heads. Albrecht, at col. 6, lines 48-50, explicitly states that Figs. 4, 5 and 6 thereof show alternative servo track patterns in accordance with its invention.

Claim 12 depends from Claim 2 as well as Claim 1, and is considered to patentably distinguish over the art for the same reasons given in support thereof. In addition, Claim 12 is considered to distinguish over the cited art in reciting reference regions that are interleaved with timing-based servo regions located on the moving storage medium, wherein the reference regions are adapted to provide information representing only the speed of the storage medium along the first direction, and the timing-based servo regions are adapted to provide information representing the position of the storage medium along a second direction perpendicular to the first direction. Neither Albrecht nor any other of the cited art shows or suggests any such features.

X. Remaining Claims Distinguish Over Cited References

Claims 14-22 respectively depend from Claim 13, and are each considered to patentably distinguish over the art for the same reasons given in support thereof.

Claim 23 is considered to patentably distinguish over the prior art, particularly in reciting reference regions that are adapted to provide information representing only the speed of the recording surface along a first direction, and timing-based servo regions that are adapted to provide information representing the position of the recording surface along a second direction perpendicular to the first direction. Such recitation is considered to distinguish over the art for reasons set forth above in regard to Claims 2 and 12.

Claims 24-29 respectively depend from Claim 23, and are each considered to patentably distinguish over the art for the same reasons given in support thereof.

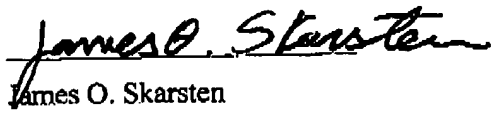
XI. Conclusion

It is respectfully urged that the subject application is patentable over the Ozdemir, Albrecht, Landman, Zortea, Contreras, Gillingham and Abe references, and over any combination thereof, and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: January 10, 2006

Respectfully submitted,



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